IN THE CLAIMS:

Please **cancel** claim 6 without prejudice.

Please amend the claims as follows.

1. (Currently amended) A multi-bit phase change memory cell, comprising:

a stack of a plurality of conductive layers including a first outer conductive layer disposed at one side of the memory cell and a second outer conductive layer disposed at a side opposite to the one side of the memory cell and a plurality of phase change material layers, each of the phase change material layers disposed between a corresponding pair of conductive layers and having electrical resistances that are different from one another, and wherein each of said plurality of phase change material layers has a different height from one another and wherein the height of each of the plurality of phase change layers increases along a direction from the first outer conductor layer to the second outer conductive layer and a surface area of each of the plurality of phase change layers decreases along the direction from the first outer conductor layer to the second outer conductive layer .

2. (Currently amended) The multi-bit phase change memory cell of claim 1, ~~the plurality of conductive layers including a first outer conductive layer disposed at one side of the memory cell and a second outer conductive layer disposed at a side opposite to the one side of the memory cell~~, wherein the electrical resistance of each of the plurality of phase change material layers ~~increasing~~ increases along ~~a~~ the direction from the first outer conductive layer to the second outer conductive layer.

3. (Original) The multi-bit phase change memory cell of claim 1, wherein each of the plurality of phase change material layers have the same resistivity.

4. (Original) The multi-bit phase change memory cell of claim 1, wherein each of the plurality of phase change material layers have a different phase transition temperature.

5. (Original) The multi-bit phase change memory cell of claim 1, wherein each of the plurality of phase change material layers have the same phase transition temperature.

6. (Canceled)

7. (Original) The multi-bit phase change memory cell of claim 1, the plurality of conductive layers including a plurality of intermediate conductive layers disposed between the first and second outer conductive layers, each of the intermediate conductive layers having the same dimensions as an adjacent phase change material layer.

8. (Original) The multi-bit phase change memory cell of claim 1, further comprising a dielectric layer formed between the first outer electrode and the second outer electrode and along sides of at least one other conductive layer and a phase change material layer disposed directly adjacent to the at least one other conductive layer.

9. (Original) The multi-bit phase change memory cell of claim 1, wherein the phase change material layers are made of the same material.

10. (Original) The multi-bit phase change memory cell of claim 1, wherein each of the phase change material layers are made of a different material.

11. (Original) The multi-bit phase change memory cell of claim 1, wherein the phase change material layers are made of $Ge_2Sb_2Te_5$.

12. (Original) The multi-bit phase change memory cell of claim 1, wherein the plurality of conductive layers are made of at least one of TiN, W, TiW, Ta, TaN, Ti, Al, Cu, and Pt.

13. (Original) The multi-bit phase change memory cell of claim 1, wherein the number of phase change material layers is equal to 2^n, where n is the number of bits stored in the memory cell.

Claims 14-21 (Canceled)

22. (Currently amended) A multi-bit phase change memory, comprising:

an array of multi-bit phase change memory cells, each of the multi-bit phase change memory cells comprising:

a stack of a plurality of conductive layers including a first outer conductive layer disposed at one side of the memory cell and a second outer conductive layer disposed at a side opposite to the one side of the memory cell and a plurality of phase change material layers, each of the phase change material layers disposed between a corresponding pair of conductive layers and having electrical resistances that are different from one another;

a programming circuit that writes data to the array of multi-bit phase change memory cells; and

a sensing circuit that reads out data from the array of multi-bit phase change memory cells, and wherein each of said plurality of phase change material layers has a different height from one another and wherein the height of each of the plurality of phase change layers increases along a direction from the first outer conductor layer to the second outer conductive layer and a surface area of each of the plurality of phase change layers decreases along the direction from the first outer conductor layer to the second outer conductive layer .

23. (Original) The method of claim 22, wherein the plurality of phase change material layers are made of $Ge_2Sb_2Te_5$.

24. (Canceled)

25. (Canceled)